Energy

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MICROCRYSTALLINE SILICON GROWTH FOR HETEROJUNCTION SOLAR CELLS

Second Quarterly Report for Period Covering April 1—June 30, 1983

By
P. A. Iles
D. C. Leung
P. H. Fang

Work Performed Under Contract No. NAS-7-100-956369

Applied Solar Energy Corporation
City Of Industry, California

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SECOND QUARTERLY REPORT

For Period Covering
1 April 1983 thru 30 June 1983

By:
P.A. Iles and D.C. Leung

and

P.H. Fang
Boston College

JPL Contract No. 956369

Applied Solar Energy Corporation
15251 E. Don Julian Road
City Of Industry, California 91746

ABSTRACT

In this reporting period, a single source of evaporation with B mixed with highly doped Si was used instead of the co-evaporation of separate Si and B sources. The purpose was to reduce possible carbon contamination. The results of both the heterojunction or heteroface structures, however, were similar to last quarter when evaporation was used. The best Voc of the heterojunction was about 460mV and no improvement in Voc in the heteroface structure, was observed; slight Voc degradation occurred. A study of the p m-Si/p c-Si structure showed a negative Voc in many cases. The highest ^{o}C voltage was up to -150mV. This indicated that the interface properties between the two materials are such that instead of repelling minority carriers from the substrate carrier, collection actually occurred. This structure defeated the purpose, but it might also mean that n-type m-Si could be beneficial and should be included in future study. Another study of cells made in the part of substrates not covered by m-Si resulted in performance lower than the controls. This indicated possible substrate degradation in the process, the extent of which wil be studied in the future.

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I. INTRODUCTION

The objective of this program is to explore the uses of microcrystal silicon (m-Si) film on single crystalline silicon (c-Si) for solar cell applications, either as a m-Si/c-Si heterojunction or using the m-Si film as a window layer to c-Si p-n junction to enhance solar cell performance. This utilization is possible because under the right circumstances m-Si has an optical bandgap of 1.7eV and potentially could enhance Voc.

The interest in m-Si lies in two areas:

a) To see if a heterojunction structure can be built which has identical lattice constants on each side of the junction.

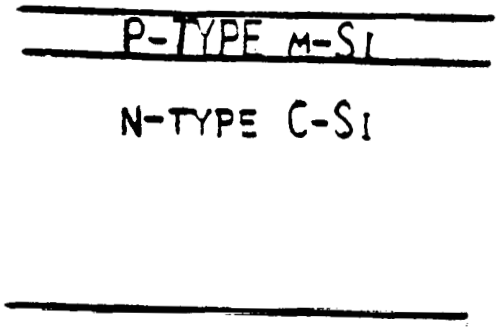
b) To see if, in a heteroface structure, the equality of lattice constants can be used to reduce surface recombination at the P+ surface in a P+/N cell (analogous to the use of AlGaAs/GaAs).

In this reporting period, a total of ten runs of film depositions was made at Boston College. The co-evaporation procedure of silicon and boron in separated boats was replaced by a single evaporation of heavily doped silicon with addition of boron, to reduce the chance of carbon contamination from the graphite boron boat. The sample structure included p mSi/n-c-Si and p mSi/n-cSi as before, but some of the substrates now had n+ back layers included to insure ohmic back contacts. Also included was a p m-Si/p c-Si structure for testing purposes. Figure 1 shows all three structures. Control cells (without the m-Si layers) were made, to assess the effect of the m-Si layer itself.

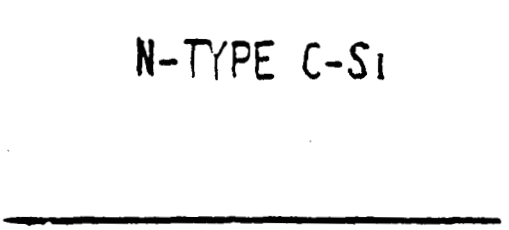
FIGURE 1

VARIOUS STRUCTURES TO BE STUDIED

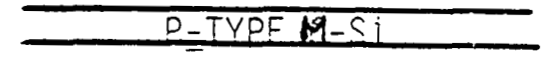
1) HETEROJUNCTION

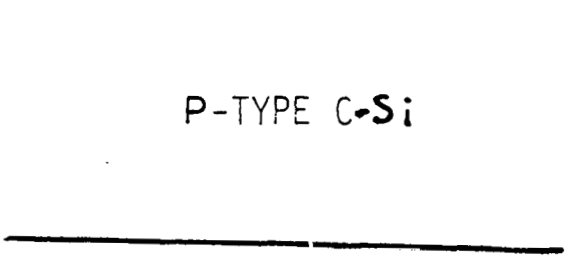


2) HETEROFACE



3) p m-Si/p c-Si TESTING STRUCTURE





II. TECHNICAL DISCUSSION

A. Change Of Evaporation Source

As mentioned in the 1st Quarterly Report, a large amount of carbon in a range of high 10^{20} to 10^{21} atoms/cm^3 was measured at JPL in m-silicon films coevaporated with boron. The carbon concentration was determined by secondary ion microscopy. The same method was also used to determine boron concentration. There are several possible sources of this carbon. One was from the contamination of diffusion oil. This possibility is unlikely on two accounts. First, the carbon concentration was excessively high. Second, the high carbon concentration occurred in the region of boron doping only. Alternatively, this carbon could come from the graphite boat of boron evaporation. There are two estimates: according to vapor pressure data, at the temperature of 1800^{o}C, the carbon vapor pressure is two orders of magnitude lower than that of boron. However, since the surface area of the high temperature region of graphite could have been appreciable, carbon vaporization could have occurred while boron was evaporated. This estimate cannot explain the observed 10 to 100 ratios of carbon concentration to boron concentration. While these conflicts are resolved, ASEC suggested evaporating p-Si from a boron doped silicon source, that is, to replace the two-source co-evaporation by a single source. The first trial with 0.1 ohm-cm silicon material gave a m-Si film of almost intrinsic conduction, implying insufficient effective boron. Following this trial, pure boron, of about .1% was mixed with silicon in a graphite crucible and heated by electron beam to the melting temperature of silicon for about 10 minutes to produce a uniform boron-silicon alloy. This source produced a suitable p-type m-Si film. Since the electron beam is located at the center of the crucible away from the graphite

crucible wall during evaporation, it is expected that graphite evaporation was minimized.

Runs 1 through 16 were made by coevaporation as reported in the 1st Quarterly Report. From 17 to the present, the new procedure to deposit p-Si was used. After two months experiments, the quality of the most recent solar cells produced by this new evaporation arrangement became as good as that by the coevaporation approach. However, a conclusion on the ultimate performance cannot be drawn yet because coevaporation procedure was backed up by several years experience, compared to only a few months with this single source procedure. Of course, it is possible that the inclusions of carbon in m-Si might not be harmful, or according to some recent results in a-Si, might even be beneficial.

B. **Solar Cell Results**

Table I summarizes the run parameters in Boston College and the results of solar cells fabricated at ASEC. All the cell parameters are listed in Appendix I. The positions of the substrates are defined as in the last report (1st Quarterly Report). Not all the samples in the runs were sent to ASEC for cell fabrication. For each sample sent, mostly four $1x1cm^2$ solar cells were fabricated. For the normal n or p-n substrates, (hence p m-Si would be deposited to form a heterojunction or window layer), those prepared after the 1st Quarter had n+ back layers to insure ohmic back contacts. The results of these p m-Si/n c-Si heterojunction or p m-Si/p-n c-Si heteroface structures were very similar to those in the 1st quarterly Report, no improvement being observed. Also p substrates with different resistivities were prepared to make p m-Si/p c-Si structures in order top study the effectiveness of the p m-Si to form a heterojunction with c-Si for testing purpose. There were very curious results for this structure. In Table 1 those ASEC substrate numbers start with a "p" were p substrates. There were quite large Voc's (~100mV) from this p m-Si/p c-Si structures, but all the measured Voc's were negative (except one substrate which produced cells with a few mV of positive voltage). This implied that instead of resisting minority carriers from the p substrate, the junctions actually collected some of them and produced negative Voc. Studies of a series of front contacts on such a substrate showed that the front contacts were ohmic and therefore were not the cause of this effect (a by product was that the sheet resistance in the film was found to be about 1000 ohm/□). If this interpretation of a carrier collecting junction is true, this could explain why no voltage enhancement as compared to control in Table 3 was achieved in the window layer structures (pm-Si/p-n-c-Si). (All the substrate numbers starting with J in Table 1 resulted in this structure). In fact there were lower Voc's in this structure which cannot be

explained by the lower current due to film absorption alone. The physical reasons for this speculation are not clear, being caused by either the interface states between m-Si and c-Si or the positions of electron affinities of m-Si and c-Si (or both). If this is the case, it is possible that the conditions that cuase negative Voc in the p m-Si/p c-Si structure could be beneficial in the n m-Si/n c-Si structure. This structure and the n m-Si/p c-Si structure will be tested. (Negative Voc's were also observed in some p m-Si/n c-Si cells in runs 17 to runs 20. This could indicate possible low doping in m-Si films in those runs. However, p m-Si/p c-Si films show negative voltage throughout).

Another test performed in this quarter was to fabricate small solar cells in the outside area of a sample not covered by the m-Si film. The original intention was to make a side by side test with cells fabricated on the film. Two pnn+ substrates were chosen for the test. The results are listed in Table 2. If Table 2 is compared with Table 3 where the results of a control run with similar substrates are summarized, it is obvious that the solar cells made on the area not covered by m-Si film in the samples were lower in both Voc and Jsc than the control*. This indicates that possibly some deterioration of substrates may have occurred during film deposition. It is not yet known whether this occurred only in the area not covered by the m-Si film or on the whole sample, because the area not covered by the m-Si film is the area which is in contact with the stainless steel of the system plate and that could be a possible source of contamination. A test is scheduled with p-n junction substrates placed in the system to undergo the temperature cycle without film deposition to see whether

*These controls were not subjected to the evaporation and hydrogenation steps.

deterioration occurs. Thus we must reduce the chance of substrate degradation by the environment in the system before checking if the problems were mainly at the interface between the m-Si and c-Si.

A supporting study in dark current measurement was conducted. Figures 2A and 2B show dark current characteristics of selected cells. Figure 1A showed heterojunction cells with high Ao (diode quantity factor) values and some series resistance. High Ao values point to interface problems in the junction. Figure 1B shows heteroface cells and their characteristics are the same as ordinary solar cells as expected.

TABLE 1

SUMMARY OF RUN CONDITIONS AND CELL RESULTS

Run	Position	ASEC#	Substrate Type	m-Si Deposition		ASEC Cells		
				Temperature (c)	Thickness (kc)	Voc(mV) Range	Jsc(mA) Range	Lot No.
17				626	2.40			
	A	40	pnn+					
	B							
	C	20	n			96-328	14.5-18.2	4
	D	70	nn+			216-316	16.6-18.2	4
	E	38	pnn+					
18				616	0.39			
	A	69	nn+			20	0.1	4
	B		p.01					
	C	21	n			100-120	1.6-4.7	
	D	J39	pn			570	19.2-19.3	4
	E	55	np					
19				621	0.49			
	A	56	nn+			1-3	0	4
	B							
	C	22	n			(3) to +2	0	4
	D	J37	pn			342-404	16.8-17.0	4
	E	56	n			(75)-(12)	(0.1)-(.7)	4
20				628	0.70			
	A	68	nn+					
	B		p.01					
	C	23	n			(52)to 2	0 to.03	4
	D	J36	pn			258-328	16.5-17.0	4
	E	57	n			(1) to 0	(0.3) to 0.1	4
21				607	.70			
	A	24	n			0	0	4
	B	J41	pn			156-168	17.6	4
	C	P1	p.15					
	D	p21	p10					
	E	p11	p2					
22				593	2.24			
	A	P2	p.15					
	B	25	n			250-326	13.0-14.7	4
	C	66	nn+			338-460	14.1-14.9	4
	D	J42	pn			564-572	14.8-15.6	4

Table 1 Cont'd.

Run	Position	ASEC#	Substrate Type	m-Si Deposition Temperature (c)	m-Si Deposition Thickness (kc)	ASEC Cells Voc(mV) Range	ASEC Cells Jsc(mA) Range	ASEC Cells Lot No.
23*				612	1.72			
	A	P28	P10					
	B	P7	P.15					
	C	P17	P2			(146)-(120)	(9.3)-(8.0)	4
	D	J45	pn			548-564	15.7-15.9	4
	E	65	nn+					
24*				623	2.35			
	A	P27	P10			(110)-(80)	(8.6)-(4.1)	4
	B	P4	P.15					
	C	P16	O2					
	D	J47						
	E	64	nn+					
25*				614	2.08			
	A	P3	P.15			(116)-(94)	(8.6)-(6.7)	4
	B	26	n			132-148	14.3-15.1	4
	C	59	n			98-112	11.8-13.9	4
	D	J43				552-558	15.1-15.3	4
	E	63	nn+					
26*				612	2.0			
	A	P8	P.15					
	B	27	n					
	C	60	n					
	D	J44	pn			554-558	14.1-14.3	4
	E	61	nn+					

All Voc and Jsc values in the parenthesis are values of the opposite polarity to what were supposed to be.

*In run 23 to 26, the boron content in p-Si source crucible has been increased.

For the P samples, the numbers that follow the letter "P" are the approximate resistivity.

None of the cells have AR coating.

1kc corresponds to about 0.3 microns in thickness.

TABLE 2

COMPARISON OF SOLAR CELLS COVERED BY m-Si WITH ADJACENT SOLAR CELLS MADE IN AREA NOT COVERED BY m-Si

		Voc (mV)	Jsc (mA/cm^2)	CFF (%)	n (%)
J-39-1 (m-Si Covered)		570	19.2	76	8.3
Adjacent Cells (Not Covered by m-Si)	a	552	20.2	63	7.0
	b	548	16.3	71	6.4
J39-2 (m-Si)		570	19.2	75	8.2
Adjacent Cells	c	550	19.2	65	6.9
	d	544	17.8	69	6.6
J39-3 (m-Si)		570	19.3	73	8.1
Adjacent Cells	e	548	17.9	71	7.1
	f	558	19.2	71	7.5
J43-1 (m-Si)		558	15.4	77	6.7
Adjacent Cells	a	552	17.5	71	6.7
	b	558	16.8	75	6.7
J43-2 (m-Si)		552	15.1	74	6.2
Adjacent Cells	c	554	18.0	74	7.5
	d	556	19.4	71	7.7
J43-3 (m-Si)		552	15.3	73	6.1
Adjacent Cells	e	552	19.1	71	7.5
	f	562	19.6	75	8.3

TABLE 3

SUMMARY OF RESULTS OF PNN+ CONTROL CELLS

	Voc (mV)	Jsc (mA/cm^2)	CFF (%)	η (%)
Average	589	22.2	73	9.6
Range	586-594	22.0-22.7	71-75	9.2-10.1

No AR coating on cells.

FIGURE 2A

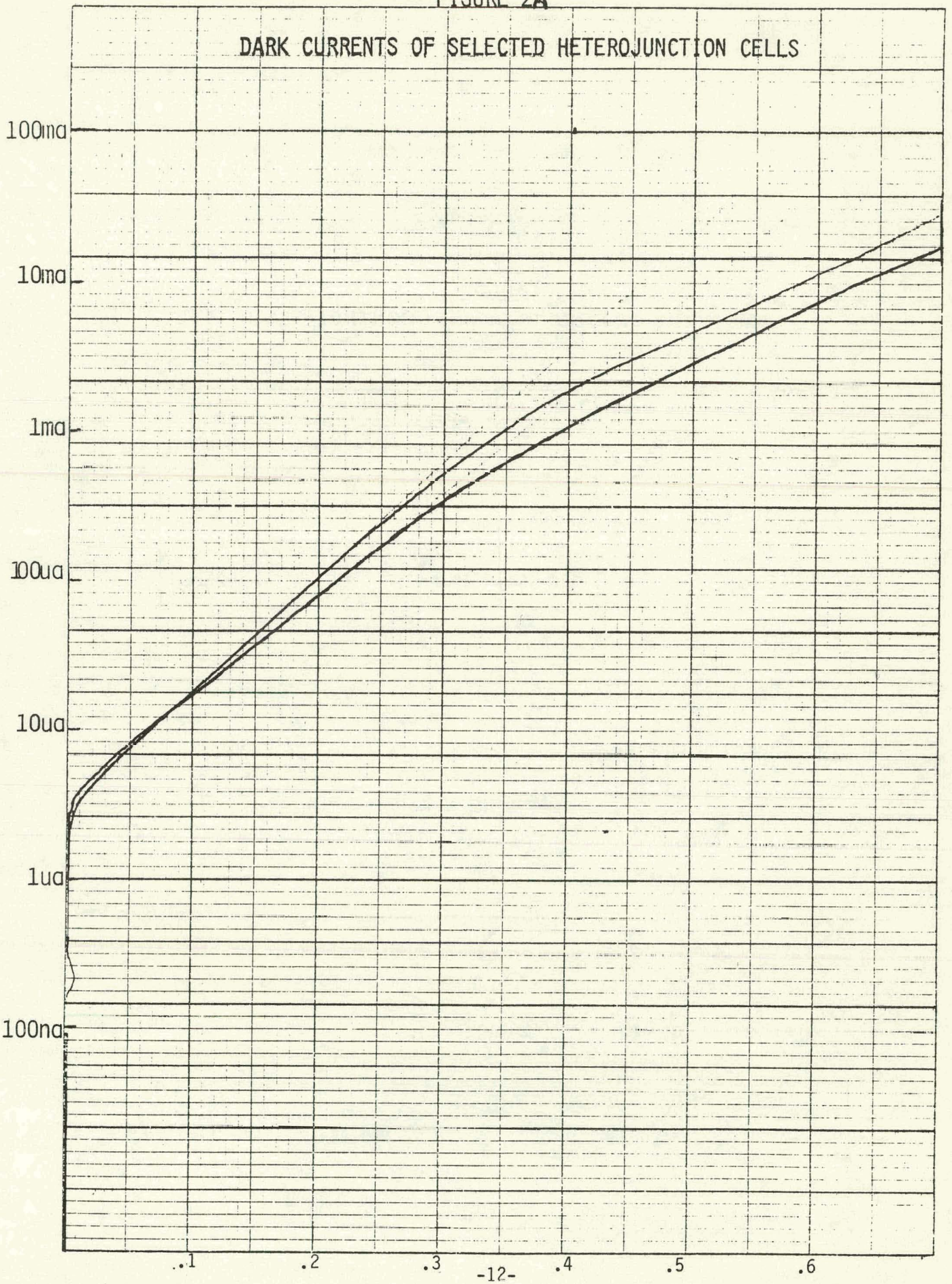
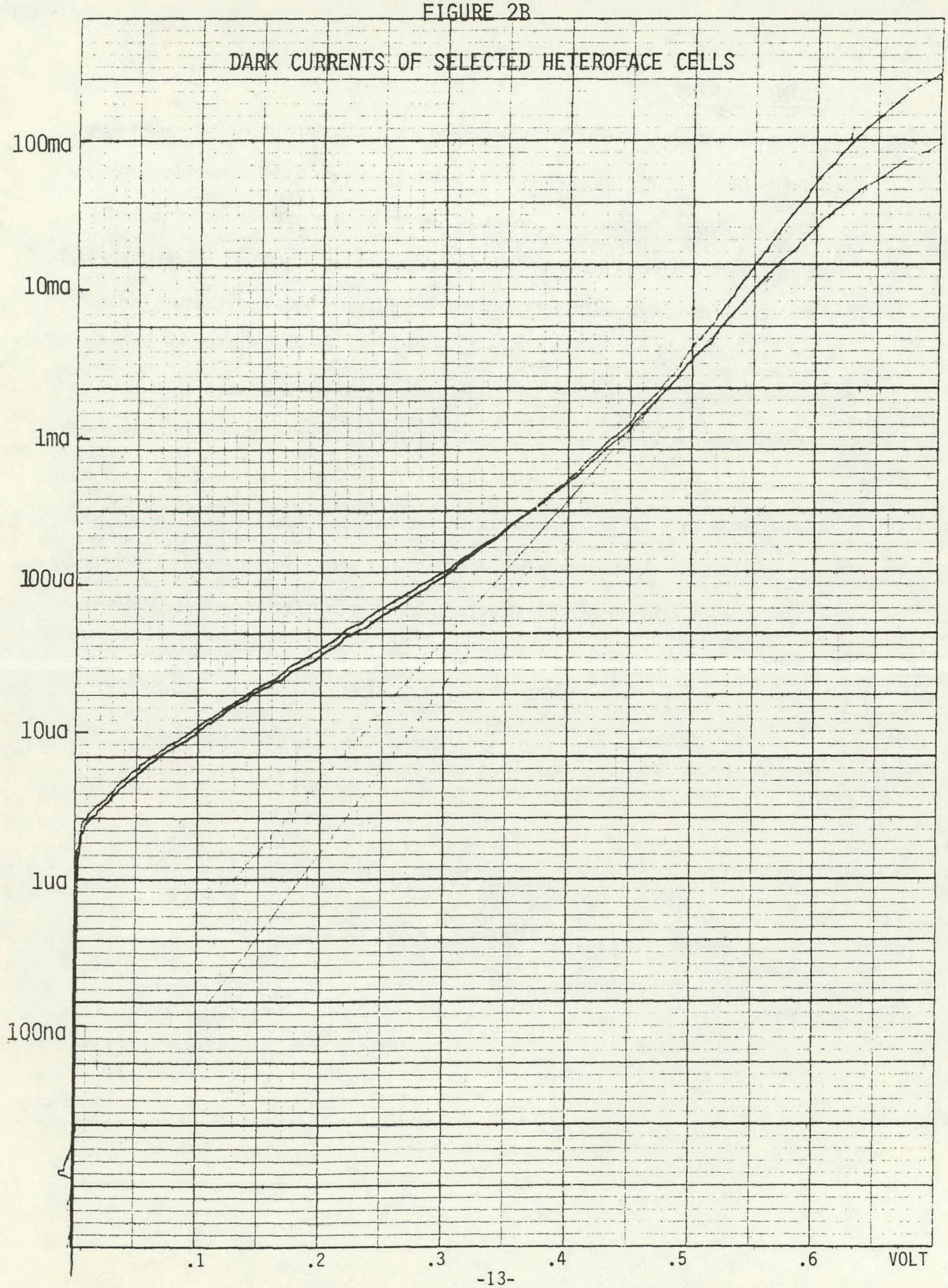

DARK CURRENTS OF SELECTED HETEROJUNCTION CELLS
100ma
10ma
1ma
100ua
10ua
1ua
100na
.1
.2
.3
.4
.5
.6

FIGURE 2B


DARK CURRENTS OF SELECTED HETEROFACE CELLS
100ma
10ma
1ma
100ua
10ua
1ua
100na
.1
.2
.3
.4
.5
.6
VOLT

III. CONCLUSIONS

Voc values in the p m-Si/n c-Si structure were still only in the high 400mV range and no improvement was yet observed in the pm-Si/p n-c-Si structure even with the new single evaporation process. Generally the optical properties of m-Si layers have not been good, and this could defeat the purpose (excessively high absorption combined with very low carrier diffusion length). Current collection was reduced but no voltage gain in either the heterojunction or heteroface structure was observed. In fact voltages were lower than control cells in both cases. Studies in the p m-Si/p c-Si structure indicate potential fundamental problems in the interface between these films and the substrates. Also solar cells made in area not covered with the samples indicate possible substrate deterioration or contamination at least in that area. Whether this is caused by local contact with the system structure, or extends to whole sample is yet to be seen.

IV. WORK PLAN STATUS

Study of p m-Si film on p c-Si and n c-Si substrates will be continued. Another test is to study the effect of the system thermal sequence on the samples. Also, tests will be conducted on low temperature annealing effects of solar cells made from the film to see if the junction properties show any improvement.

APPENDIX I

INDIVIDUAL CELL DATA

SOLAR CELL ELECTRICAL DATA

CELL DESCRIPTION: Heterojunction p msi / n c-Si cells

TEST CONDITION: ~~25~~ AM1 no AR
TEMPERATURE: 28°C

NO.	V_{OC} mV	J_{SC} mA/cm^2	P_{Max} mW	CFF %	n %	AREA cm^2
20-1	254	17.5		51	2.3	
2	328	18.2		55	3.2	
3	218	18.0		48	1.9	
4	96	14.5		24	0.3	
21-1	100	1.6		24	—	
2	102	1.6		24	—	
3	130	~~3~~3.7		23	0.1	
4	120	4.7		23	0.1	
22-1	0	0				
22-2	-3	0				
22-4	~~+2~~ +2	0				
23-1	2	0.3				
-2	0	0				
-3	-42	0				
-4	-52	0				
24-3	0	0				
24-4	0	0				

SOLAR CELL ELECTRICAL DATA

CELL DESCRIPTION: (Continue) Hetrojunction P m-Si / n·c-Si

TEST CONDITION: Am1 no AR
TEMPERATURE 28°C

NO.	V_{OC}	J_{SC}	P_{Max}	CFF	n	AREA
	mV	mA/cm^2	mW	%	%	cm^2
25-1	326	14.7		38	1.8	
25-2	298	13.0		33	1.3	
25-3	250	14.7		31	1.2	
25-4	298	14.7		40	1.7	
26-1	132	14.3		37	0.7	
2	148	15.1		39	0.9	
3	146	14.9		38	0.8	
4	140	14.7		38	0.8	
56-1	-51	-0.1				
2	-12	0				
3	-75	-0.2				
4	-19	-0.7				
57-1	-1	-0.1				
2	-1	-0.3				
3	0	+0.1				
4	0	0				

SOLAR CELL ELECTRICAL DATA

CELL DESCRIPTION: (Continue) Hetro-function P m-Si / n c-Si

TEST CONDITION: AM1 no AR

TEMPERATURE: 28°C

NO.	V_{OC} mV	J_{SC} mA/cm^2	P_{Max} mW	CFF %	n %	AREA cm^2
59-1	112	13.9		35	0.6	
-2	106	13.3		34	0.5	
-3	100	12.4		31	0.4	
-4	98	11.8		29	0.3	
66-1	388	14.1		56	3.1	
2	408	14.1		50	2.9	
3	456	14.7		56	3.8	
4	460	14.9		63	4.3	
67-1	3	0				
2	2	0				
3	1	0				
4	1	0				
69-1	20	0				
69-2	20	0.1				

SOLAR CELL ELECTRICAL DATA

CELL DESCRIPTION: (continue) · Hetrojunction P a-Si / n c-Si

TEST CONDITION: AM1 no AR

TEMPERATURE: 28°C

NO.	V_{OC}	J_{SC}	P_{Max}	CFF	n	AREA
	mV	mA/cm^2	mW	%	%	cm^2
70-1	240	17.3		42	1.7	
2	216	16.6		39	1.4	
3	240	17.7		39	1.6	
4	316	18.2		47	2.7	

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SOLAR CELL ELECTRICAL DATA

CELL DESCRIPTION: Hetroface p m-Si./p-n c-Si

TEST CONDITION: AM1 NO AR coating

TEMPERATURE: 28°C

NO.	V_{OC}	J_{SC}	P_{Max}	CFF	n	AREA
	mV	mA/cm^2	mW	%	%	cm^2
J36-1	328	17.0		56	3.1	
2	296	16.5		57	2.8	
3	274	16.5		59	2.7	
4	258	16.8		58	2.5	
J37-1	404	17.0		51	3.5	
2	376	16.8		55	3.5	
3	354	17.0		54	3.2	
4	342	16.8		43	2.5	
J39-1	570	19.2		76	8.3	
2	570	19.2		75	8.2	
3	570	19.3		73	8.1	
J41-1	168	17.6		48	1.4	
	156	17.6		46	1.3	
J42-1	564	14.8		74	6.2	
2	568	15.3		76	6.6	
3	570	15.6		76	6.7	
4	572	15.6		74	6.6	

SOLAR CELL ELECTRICAL DATA

CELL DESCRIPTION: (Continue) Hetroface p mSi / p-n c-Si

TEST CONDITION: AM1 no AR
TEMPERATURE: 28°C

NO.	V_{OC}	J_{SC}	P_{Max}	CFF	n	AREA
	mV	mA/cm^2	mW	%	%	cm^2
J43-1	558	15.4		77	6.7	
2	552	15.1		74	6.2	
3	552	15.3		73	6.1	
J44-1	556	14.1		75	5.9	
2	554	14.1		74	5.8	
3	558	14.1		76	6.0	
4	556	14.3		75	6.0	
J45-1	564	15.9		77	6.9	
2	562	15.7		78	6.9	
3	558	15.4		73	6.5	
4	548	15.8		71	6.2	

SOLAR CELL ELECTRICAL DATA

CELL DESCRIPTION: P/p p.msi/p-si Testing structures

TEST CONDITION: ~~[illegible]~~ AM1 NO AR
TEMPERATURE: 28°

NO.	V_{OC}	J_{SC}	P_{Max}	CFF	n	AREA
	mV	mA/cm^2	mW	%	%	cm^2
P 3-1	-112	-6.7				
P 3-2	-116	-8.6				
P 3-3	-106	-8.2				
P 3-4	-94	-8.3				
P 7-1	6	0.3				
P 7-2	5	0.3				
P 7-3	4	0.3				
P 7-4	0	0				
P 8-1	-84	-6.7				
P 8-2	-94	-6.7				
P 8-3	-86	-5.3				
P 8-4	-92	-4.3				
P 17-1	-120	-8.0				
17-2	-140	-9.3				
P 17-3	-146	-9.0				

SOLAR CELL ELECTRICAL DATA

CELL DESCRIPTION: (Continue) P m-Si / P c-Si Testing Structure

TEST CONDITION: AM1 No AR Coating
TEMPERATURE 28°c

NO.	V_{OC}	J_{SC}	P_{Max}	CFF	n	AREA
	mV	mA/cm^2	mW	%	%	cm^2
P 27-1	-110	-8.5				
P 27-2	-104	-8.6				
P 27-3	-88	-6.7				
P 27-4	-80	-4.1				

SOLAR CELL ELECTRICAL DATA

CELL DESCRIPTION: W-Si on P/N junction cells (J 39-1, 2, 3) with adjacent P/N cells without m-Si on 52Ω same substrate (a, b, c, d, e, f)

TEST CONDITION: AM1 no AR

TEMPERATURE: 28°C

NO.	V_{OC}	J_{SC}	P_{Max}	CFF	η	AREA
	mV	mA/cm^2	mW	%	%	cm^2
J39-1	570	19.2		76	8.3	
a	552	20.2		63	7.0	
b	548	16.3		71	6.4	
J39-2	570	19.2		75	8.2	
c	550	19.2		65	6.9	
d	544	17.8		69	6.6	
J39-3	570	19.3		73	8.1	
e	548	17.9		71	7.1	
f	558	19.2		71	7.5	

SOLAR CELL ELECTRICAL DATA

CELL DESCRIPTION: M-Si on P/N junction cells (J43-1, 2, 3) with adjacent P/N cells without M-Si on the same substrate (a, b, c, d, e, f)

TEST CONDITION: AM1 no AR

TEMPERATURE: 28°C

NO.	V_{OC}	J_{SC}	P_{Max}	CFF	n	AREA
	mV	mA/cm^2	mW	%	%	cm^2
J43-1	~~558~~	15.4		77	6.7	
a	552	17.5		71	6.7	
b	558	16.8		75	6.7	
J43-2	552	15.1		74	6.2	
c	554	18.0		74	7.5	
d	556	19.4		71	7.7	
J43-3	552	15.3		73	6.1	
e	552	19.1		71	7.5	
f	562	19.6		75	8.3	

SOLAR CELL ELECTRICAL DATA

CELL DESCRIPTION: PNN+ control

TEST CONDITION: AM1 .. 2.2 AR

TEMPERATURE: 28°C

NO.	V_{OC}	J_{SC}	P_{Max}	CFF	n	AREA
	mV	mA/cm^2	mW	%	%	cm^2
1	588	22.1		74	9.6	4
2	587	22.0		71	9.2	4
3	586	22.0		72	9.3	4
4	594	22.7		75	10.1	4

APPENDIX II

TIME SCHEDULE

TIME SCHEDULE